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Design of Baugh-wooley Multiplier using Verilog HDL

Shruti D. Kale, Prof. Gauri N. Zade
India

Abstract: **-** Multiplication represents one of the major holdups in most digital signal processing system. With advances in technology, many researchers have tried and are trying to design multipliers which offer high speed, low power consumption and hence less area in one multiplier thus making them suitable for various high speed, low power and compact implementation. To achieve speed improvementsBaugh Wooley Multiplication technique used for signed multiplication. It is not widely used because of its complexity of its structure. This paper examines the number of LUT's used by the design from available quantity along with the analysis of IOB's and slices for related & unrelated logic are done.

I. INTRODUCTION

The prolific growth in semiconductor device industry has led to the advancement of high performance portable systems with heighten reliability in data transmission. Multiplication is a heavily used arithmetic operation that figures distinguished in signal processing and scientific applications. Typical DSP applications where a multiplier plays an important role include digital filtering, digital communications and spectral analysis. Many current DSP applications are aimed at portable, battery-operated systems, so that power dissipation becomes one of the primary design limitations. Meanwhile multipliers are quite complex circuits and must typically operate at a high system clock rate, dropping the delay of a multiplier is a vital part of satisfying the overall design.

The ALU is the core in DSP and ASIC where it is used in comparison, convolution, correlation, and digital filters. An ALU combines a variety of arithmetic and logic operations into a single unit. The speed of ALU greatly depends on its multiplier circuit. This in turn increase demand for high speed multipliers, at the same time keeping in mind low area and moderate power consumption. Generation of partial product and their accumulation are the two basic operation of multiplication. A binary multiplier is an electronic circuit used in digital electronics, like a computer to multiply two binary numbers. There are different types of multiplier.

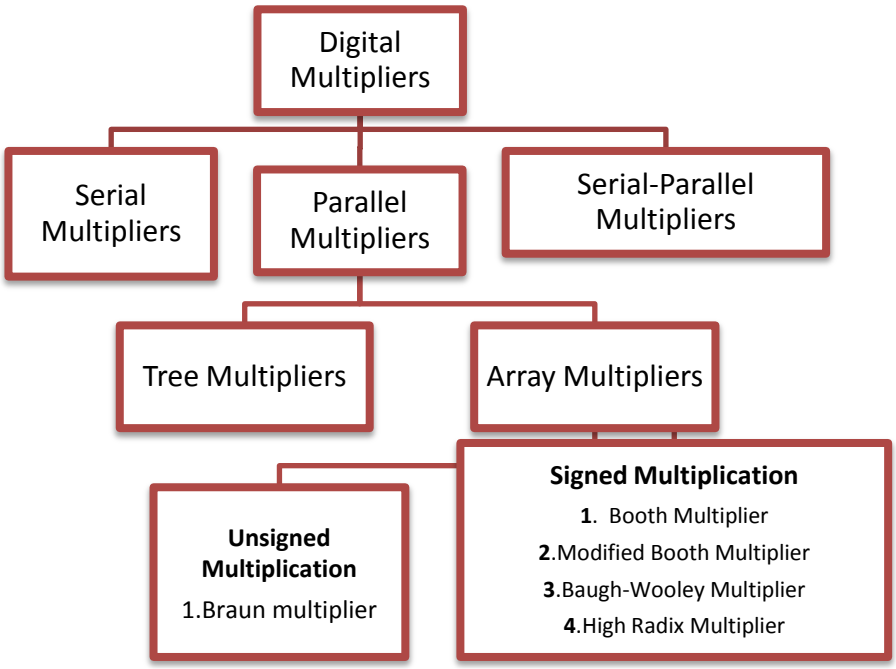

Fig: Classification of Digital Multipliers

II. LITERATURE REVIEW

Charles R. Baugh and Bruce A. Wooley, member of IEEE presents "A Two's complement parallel Array Multiplication Algorithm" in 1973. In this two's complement, m-bit by n-bit parallel array multiplication is described. As multiplication is an essential function in digital system due to its necessity in operation of digital filters and Fourier transform processor. This paper presents an algorithm for parallel two's complement multiplication. The advantage of the algorithm is the sign of all the partial products bits are positive, which allow the product to be formed using array addition technique. The drawback of the proposed algorithm is the need for the complements of each multiplier and multiplicand bit.[4]

AswathySudhakar et al in 2010 proposed "High Speed Power-Efficient Modified Baugh-Wooley Multipliers", in this in this they proved modified Baugh-Wooley multiplier. Here comparison of various multiplier architecture for VLSI application. The baugh-wooley multiplier found to be best suited for the multiplication functionality according to resolution and efficiency.[1]

K'Andrea et al presents, "Analysis of column compression multipliers" in 2001. This paper tests the proficiency of the area, delay and power characteristic of Dadda and Wallace multiplier. As operand word length increases, column compression multiplier increases roughly. Simulation indicate that, Wallace multipliers have 4% to 7% more area than equivalent Dadda multiplier, and approximately the same delay for operand sizes from 8 to 64 bits. [5]

Andrew D. Booth present "A signed binary multiplication technique". In this a technique is described by which binary numbers of either sign may be multiplied together by a uniform process which is independent. In the design of automatic computing machines it is necessary to have two numbers whose signs are not necessarily positive. [6]

III. SYSTEM MODEL DESCRIPTION

The array multiplier Baugh-Wooley is an efficient way for multiplying both signed and unsigned numbers. Baugh Wooley algorithm is used in High Performance Multiplier (HPM) tree, which inherits regular and repeating structure of the array multiplier. Baugh Wooley multiplier exhibits less delay, low power dissipation and the area occupied is also small compared to other array multipliers. The architecture of Baugh Wooley multiplier is based on carry save algorithm.

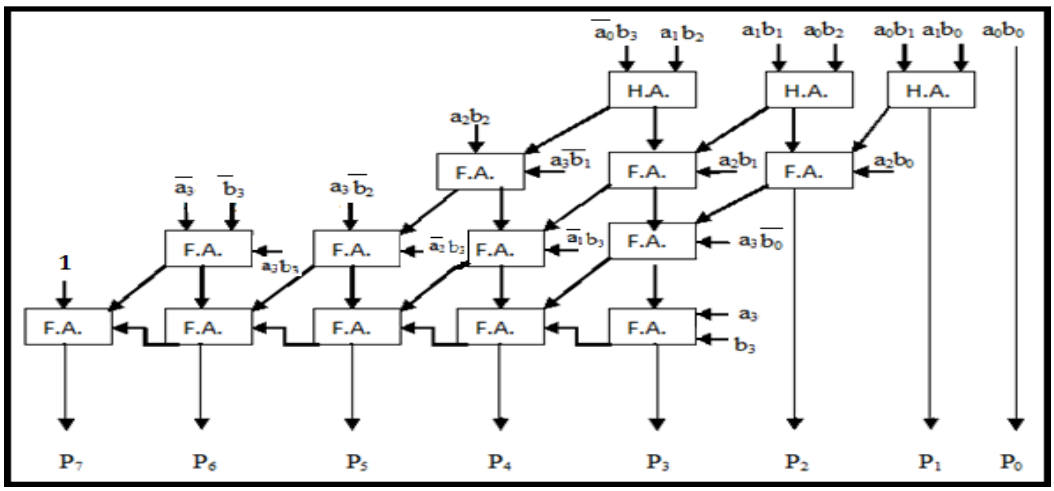

Fig. 3: Baugh-wooley multiplier Archicture

IV. WORKING

The multiplication algorithm can be represented as shown below. Here, two 4 bit numbers are multiplied using Baugh Wooley algorithm, and the partial products are given by Pp0 to Pp6 the MSB bits are signed bits and are represented using "bar".

b_3	b_2	b_1	b_0				
a_3	a_2	a_1	a_0				
			$(a_0 b_3)$	$(a_0 b_2)$	$(a_0 b_1)$	$(a_0 b_0)$	
		$(a_1 b_3)$	$(a_1 b_2)$	$(a_1 b_1)$	$(a_1 b_0)$	x	
	$(a_2 b_3)$	$(a_2 b_2)$	$(a_2 b_1)$	$(a_2 b_0)$	x	x	
$(a_3 b_3)$	$(a_3 b_2)$	$(a_3 b_1)$	$(a_3 b_0)$	x	x	x	
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Addition of Positive products:-

				(a_0b_2)	(a_0b_1)	(a_0b_0)
			(a_1b_2)	(a_1b_1)	(a_1b_0)	x
(a_3b_3)	0	(a_2b_2)	(a_2b_1)	(a_2b_0)	x	x

Addition of Negative products:-

0	0	(a_3b_2)	(a_3b_1)	(a_3b_0)
0	0	(a_2b_3)	(a_1b_3)	(a_0b_3)
a_3	$\overline{a_3}$	$a_3\overline{b_2}$	$a_3\overline{b_1}$	$a_3\overline{b_0}$
				a_3
b_3		$\overline{a_2}b_3$	$\overline{a_1}b_3$	$\overline{a_0}b_3$
				b_3

$$-128\,a_3+64\,a_3 = -64\,a_3$$
$$= 64(\overline{a_3}-1)$$

Similarly,

$$-128\,b_3+64\,b_3 = -64\,b_3$$
$$= 64(\overline{b_3}-1)$$

Therefore,

$$64\,\overline{a_3} + 64\,\overline{b_3} - 128$$

Signed bits can be multiplied using this algorithm, where all numbers are represented in their 2's complement form for this the architecture is slightly modified by adding an XOR gate, the input is 1st given to the XOR gate, thus converting the number to its 2's complement form. The XOR gate has the multiplicand as one input and a control line which is connected to an enable as another input. When the enable line goes high the XOR gates invert the input add a 1 to the bits resulting in the 2's complement of the number. When the enable line is low the bit is passed as such without any inversion. Here a simple circuit of Baugh Wooley is given for multiplication of signed numbers.

V. RESULT

RTL Schematic:-

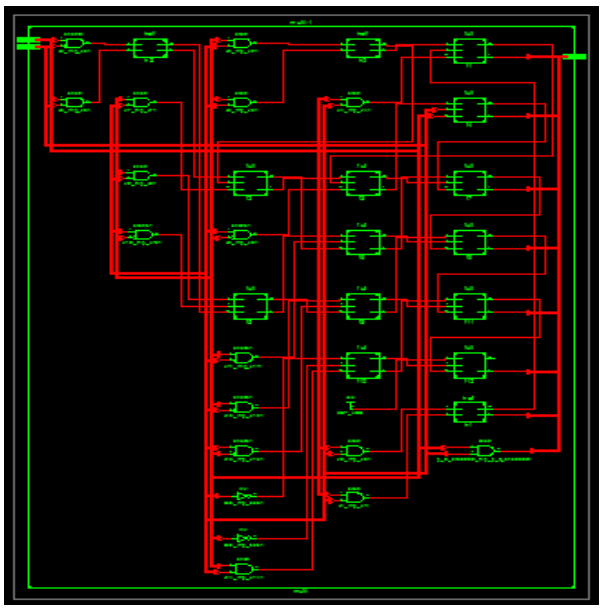

Fig. 4: RTL Schematic of Baugh-Wooley Multiplier

Technology schematic:-

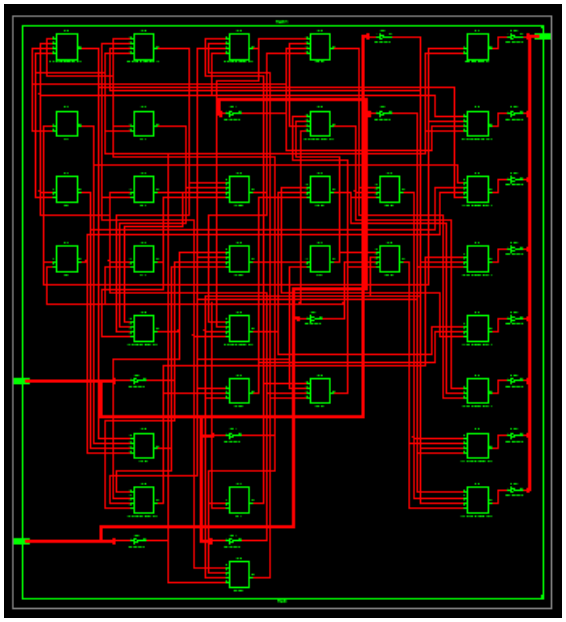

Fig. 5: Technology Schematic of Baugh-Wooley Multipler

Simulation Result:-

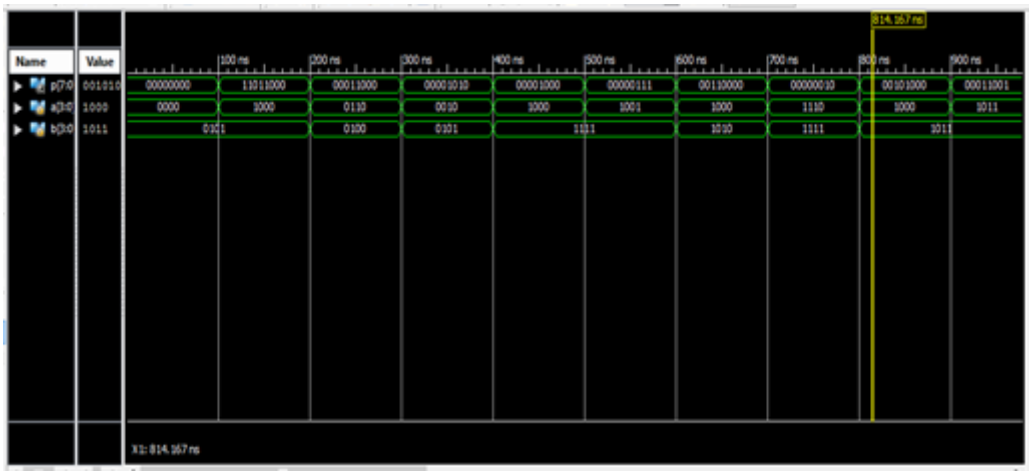

Fig. 6: Simulation Result of Baugh-Wooley Multiplier

Fig. 4 shows the resulted RTL schematic for Baugh-Wooley multiplier. The fig. 5 shows the technical schematic for Baugh-Wooley multiplier. Fig. 6 shows simulation result for Baugh-Wooley multiplier.
Device utilization summary:-

Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	33	11,776	1%
Number of occupied Slices	18	5,888	1%
Number of Slices containing related logic	18	18	100%
Number of Slices containing unrelated logic	0	18	0%
Total Number of 4 input LUTs	33	11,776	1%
Number of Bonded IOBs	16	372	4%

VI. CONCLUSION

In this paper Baugh-Wooley multiplier architecture has been discussed. It is observed that Baugh-Wooley architecture is faster in performance as compared to other conventional multiplier and hence suited for reconfiguration.

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